EE 505
Assignment 1
Spring 2023
Due Wednesday Feb 1

Problem 1 There are a small number of different ADC architectures that dominate the commercial catalog parts that are available today. The dominant architectures are SAR, Pipelined, and Delta-Sigma. Speed and resolution are the driving factors that dictate which architecture is most suitable though the process node may affect the tradeoffs. The figure below (extracted from a TI presentation) shows the conventional wisdom of which structures are best suited for different applications. Though not explicitly shown in this figure, power dissipation and cost are also important factors in determining the most suitable architecture for a given application. Listings of the general purpose ADCs available from TI and Analog Devices (ADI) are included in the linked spreadsheet. From these spreadsheets, create a method of graphically showing how the breakdown between these different architectures occurs. In this comparison the number of data converters in each part of the resolution/conversion rate planes should be appropriately represented.

Note 1: The ENOB from an INL viewpoint is given for most (but not all) of the architectures in the spreadsheets so repeat your assessment by correcting the specified resolution (n_R) by the relationship given below when making this comparison.

$$n_{EFF} = n_R - 1 - \log_2(\upsilon)$$

In this equation, v is the INL in LSB. So, for example, if n_R=14 and v=4, n_{EFF}=11.

Some commercial die will be given different part numbers with slightly different specifications. These parts may be over-represented in your comparison but there is probably not an easy way to identify those parts from the data available in the spreadsheet.

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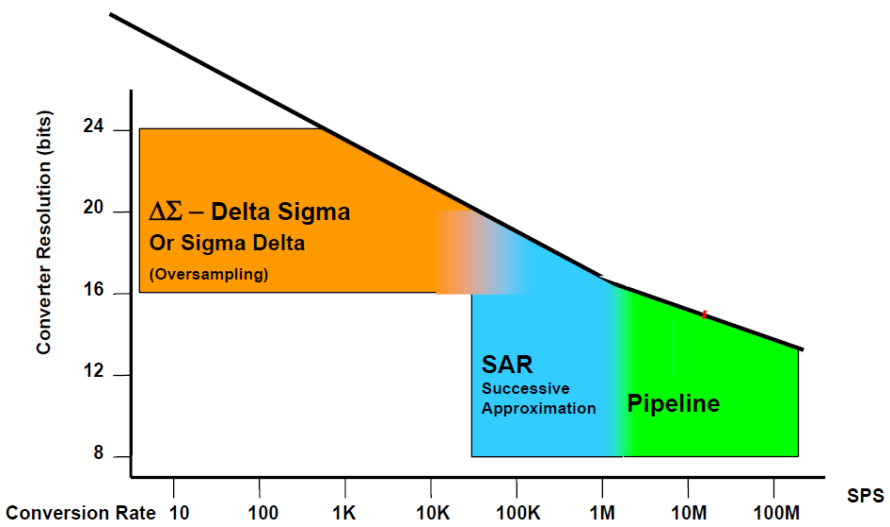

Problem 2 Power is often of considerable concern when specifying an ADC. Increases in resolution and increases in conversion rate invariably require more power but this relationship is highly nonlinear.

Based upon the spreadsheets that are linked, develop a model that relates resolution, conversion rate, and power dissipation and make a comparison of how the devices fit in this model. (Note: you may need to change the units in the speed column before doing sorts to be sure all are consistent). Based upon your model, identify outliers that are most attractive and outliers that are least attractive. Is there any significant difference in performance between the two major manufacturers?

Problem 3 This is closely related to Problem 2. Many journal and conference papers use as a figure of merit $F = \frac{P}{f_S 2^{n_{EFF}}}$ where f_S is the sampling rate and n_{EFF} is the effective resolution (or ENOB). The goal with this figure of merit is to have a figure of merit that is unaffected by P, f_S, and n_{EFF}. Following this thought process, a good design will have a low value for F and presumably good parts throughout the f_S-resolution plane will all have the same value of F.

a) Compute F for the commercial parts listed in the spreadsheets.
b) Is this figure of merit independent of f_S and n ?
c) Identify 5 ADCs that have appeared in either ISSCC or the IEEE Journal of Solid State Circuits in the past 12 months and compare F for these circuits to what is actually commercially available from Analog Devices. Comment on your observations.
d) How does F compare between the two major ADC companies, TI and ADI?